a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

I 1 End

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate; and

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate.

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21. (Amended) An active matrix liquid crystal display comprising:

I 2

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

B1+ a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate; and

I 2 Cont'd

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate.

22. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate, said sealing material being provided outside at least said pixel TFTs; and

#17

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate.

I2 cont'd

23. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate, said sealing material being provided outside at least said pixel TFTs; and

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate.

24. (Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

I2 is cont'd

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate and outside at least said pixel TFTs; and

#25

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate,

said method comprising

cutting said first substrate and said counter substrate outside said sealing material having said control circuit under and in contact with said sealing material.

25. (Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

I2 End

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate; and

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate,

said method comprising:

cutting said first substrate and said counter substrate outside said sealing material having said control circuit under and in contact with said sealing material.

I3

61. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

I3 Cont'd

a sealing material provided between said first substrate and said counter substrate; and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

62. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

63. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said first substrate;

I3 Cont'd

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

64. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said first substrate;

a counter substrate located opposite to said first substrate;

I3 Cont'd

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.